**MICROPOWER PHASE-LOCKED LOOP**

- **QUIESCENT CURRENT SPECIFIED UP TO 20V**
- **VERY LOW POWER CONSUMPTION**: 70µW (TYP.) AT VCO \( f_0 = 10\text{kHz}, V_{DD} = 5\text{V} \)
- **OPERATING FREQUENCY RANGE**: UP TO 1.4MHz (TYP.) AT \( V_{DD} = 10\text{V} \)
- **LOW FREQUENCY DRIFT**: 0.04%/°C (typ.) AT \( V_{DD} = 10\text{V} \)
- **CHOICE OF TWO PHASE COMPARATORS**:
  1) EXCLUSIVE - OR NETWORK
  2) EDGE-CONTROLLED MEMORY NETWORK WITH PHASE-PULSE OUTPUT FOR LOCK INDICATION
- **HIGH VCO LINEARITY**: <1% (TYP.)
- **VCO INHIBIT CONTROL FOR ON-OFF KEYING AND ULTRA-LOW STANDBY POWER CONSUMPTION**
- **SOURCE-FOLLOWER OUTPUT OF VCO CONTROL INPUT (demod. output)**
- **ZENER DIODE TO ASSIST SUPPLY REGULATION**
- **5V, 10V AND 15V PARAMETRIC RATINGS**
- **INPUT LEAKAGE CURRENT**
  \( I_I = 100nA \) (MAX) AT \( V_{DD} = 18\text{V}, T_A = 25^\circ\text{C} \)
- **100% TESTED FOR QUIESCENT CURRENT**
- **MEETS ALL REQUIREMENTS OF JEDEC JESD13B "STANDARD SPECIFICATIONS FOR DESCRIPTION OF B SERIES CMOS DEVICES"**

**ORDER CODES**

<table>
<thead>
<tr>
<th>PACKAGE</th>
<th>TUBE</th>
<th>T &amp; R</th>
</tr>
</thead>
<tbody>
<tr>
<td>DIP</td>
<td>HCF4046BEY</td>
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</tr>
<tr>
<td>SOP</td>
<td>HCF4046BM1</td>
<td>HCF4046M013TR</td>
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**DESCRIPTION**

The HCF4046B is a monolithic integrated circuit fabricated in Metal Oxide Semiconductor Technology, available in 16-lead dual in-line plastic or ceramic package. The HCF4046B CMOS Micropower Phase-Locked Loop (PLL) consists of a low-power, linear voltage-controlled oscillator (VCO) and two different phase comparators having a common signal-input amplifier and a common comparator input. A 5.2V zener diode is provided for supply regulation if necessary.

**PIN CONNECTION**

- **PHASE PULSES**
- **PHASE COMP I OUT**
- **COMPONATOR IN**
- **VCO OUT**
- **INHIBIT**
- **C1**
- **VSS**
- **VDD**
- **ZENER**
- **SIGNAL IN**
- **PHASE COMP II OUT**
- **R2 TO VSS**
- **R1 TO VSS**
- **DEMODULATOR OUT**
- **VCO IN**
VCO Section

The VCO requires one external capacitor C1 and one or two external resistors (R1 or R1 and R2). Resistor R1 and capacitor C1 determine the frequency range of the VCO and resistor R2 enables the VCO to have a frequency offset if required. The high input impedance ($10^{12}\,\Omega$) of the VCO simplifies the design of low-pass filters by permitting the designer a wide choice of resistor-to-capacitor ratios. In order not to load the low-pass filter, a source-follower output of the VCO input voltage is provided at terminal 10 (DEMODULATED OUTPUT). If this terminal is used, a load resistor ($R_S$) of 10 KΩ or more should be connected from this terminal to $V_{SS}$. If unused this terminal should be left open. The VCO can be connected either directly or through frequency dividers to the comparator input of the phase comparators. A full CMOS logic swing is available at the output of the VCO and allows direct coupling to CMOS frequency dividers such as the HCF4024B, HCF4018B, HCF4020B, HCF4022B, HCF4029B and HBF4059A. One or more HCF4018B (Presetable Divide-by-N Counter) or HCF4029B (Presetable Up/Down Counter), or HBF4059A (Programmable Divide-by-"N" Counter), together with the HCF4046B (Phase-Locked Loop) can be used to build a micropower low-frequency synthesizer. A logic 0 on the INHIBIT input "enables" the VCO and the source follower, while a logic 1 "turns off" both to minimize stand-by power consumption.

Phase Comparators

The phase-comparator signal input (terminal 14) can be direct-coupled provided the signal swing is within CMOS logic levels [logic "0" $\leq 30\%$ of ($V_{DD}-V_{SS}$), logic "1" $\geq 70\%$ of ($V_{DD}-V_{SS}$)]. For smaller swings the signal must be capacitively coupled to the self-biasing amplifier at the signal input. Phase comparator I is an exclusive-OR network; it operates analogously to an over-driven balanced mixer. To maximize the lock range, the signal-and comparator-input frequencies must have a 50% duty cycle. With no signal or noise on the signal input, this phase comparator has an average output voltage equal to $V_{DD}/2$. The low-pass filter connected to the output of phase comparator I supplies the averaged voltage to the VCO input, and causes the VCO to oscillate at the center frequency ($f_0$). The frequency range of input signals on which the PLL will lock if it was initially out of lock is defined as the frequency capture range ($2f_C$). The frequency range of input signals on which the loop will stay locked if it was initially in lock is defined as the frequency lock range ($2f_L$). The capture range is $\leq$ the lock range. With phase comparator I the range of frequencies over which the PLL can acquire lock (capture range) is dependent on the low-pass-filter characteristics, and can be made as large as the lock range. Phase-comparator I enables a PLL system to remain in lock in spite of high amounts of noise in the input signal. One characteristic of this type of phase comparator is that it may lock onto input frequencies that are close to harmonics of the VCO center-frequency. A second characteristic is that the phase angle between the signal and the comparator input varies between 0° and 180°, and is 90° at the center frequency. Fig.1 shows the typical, triangular, phase-to-output response characteristic of phase-comparator I. Typical waveforms for a CMOS phase-locked-loop employing phase comparator I in locked condition of $f_0$ is shown in fig.2. Phase-comparator II is an edge-controlled digital memory network. It consists of four flip-flop stages, control gating, and a three-stage output-circuit comprising p- and n-type drivers having a common output node. When the p-MOS or n-MOS drivers are ON they pull the output up to $V_{DD}$ or down to $V_{SS}$, respectively. This type of phase comparator acts only on the positive edges of the signal and comparator inputs. The duty cycles of the signal and comparator inputs are not important since positive transitions control the PLL system utilizing this type of comparator. If the signal-input frequency is higher than the comparator-input frequency, the p-type output driver is maintained ON most of the time, and both the n- and p-drivers OFF (3 state) the remainder of the time. If the signal-input frequency is lower than the comparator-input frequency, the n-type output driver is maintained ON most of the time, and both the n- and p-drivers OFF (3 state) the remainder of the time. If the signal and comparator-input frequencies are the same, but the signal input lags the comparator input in phase, the n-type output driver is maintained ON for a time corresponding to the phase difference. If the signal and comparator-input frequencies are the same, but the comparator input lags the signal in phase, the
p-type output driver is maintained ON for a time corresponding to the phase difference. Subsequently, the capacitor voltage of the low-pass filter connected to this phase comparator is adjusted until the signal and comparator inputs are equal in both phase and frequency. At this stable point both p- and n-type output drivers remain OFF and thus the phase comparator output becomes an open circuit and holds the voltage on the capacitor of the low-pass filter constant. Moreover the signal at the "phase pulses" output is a high level which can be used for indicating a locked condition. Thus, for phase comparator II, no phase difference exists between signal and comparator input over the full VCO frequency range. Moreover, the power dissipation due to the low-pass filter is reduced when this type of phase comparator is used because both the p- and n-type output drivers are OFF for most of the signal input cycle. It should be noted that the PLL lock range for this type of phase comparator is equal to the capture range, independent of the low-pass filter. With no signal present at the signal input, the VCO is adjusted to its lowest frequency for phase comparator II. Fig.3 shows typical waveforms for a CMOS PLL employing phase comparator II in a locked condition.

**Figure 1**: Phase-Comparator I Characteristics at Low-Pass Filter Output.

![Figure 1](image1)

**Figure 2**: Typical Waveforms for CMOS Phase Locked-Loop Employing Phase Comparator I in Locked Condition of \( f_0 \).
Figure 3: Typical Waveforms for CMOS Phase-locked Loop Employing Phase Comparator II In Locked Condition

**INPUT EQUIVALENT CIRCUIT**

**PIN DESCRIPTION**

<table>
<thead>
<tr>
<th>PIN No</th>
<th>SYMBOL</th>
<th>NAME AND FUNCTION</th>
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<tbody>
<tr>
<td>1</td>
<td>PHASE PULSES</td>
<td>Phase Comparator Pulse Output</td>
</tr>
<tr>
<td>2</td>
<td>PHASE COMP I OUT</td>
<td>Phase Comparator 1 Output</td>
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<tr>
<td>3</td>
<td>COMPARATOR IN</td>
<td>Comparator Input</td>
</tr>
<tr>
<td>4</td>
<td>VCO OUT</td>
<td>VCO Output</td>
</tr>
<tr>
<td>5</td>
<td>INHIBIT</td>
<td>Inhibit Input</td>
</tr>
<tr>
<td>6, 7</td>
<td>C1</td>
<td>Capacitors</td>
</tr>
<tr>
<td>9</td>
<td>VCO IN</td>
<td>VCO Input</td>
</tr>
<tr>
<td>10</td>
<td>DEMODULATOR OUT</td>
<td>Demodulator Output</td>
</tr>
<tr>
<td>11</td>
<td>R1 TO VSS</td>
<td>Resistor R1 Connection</td>
</tr>
<tr>
<td>12</td>
<td>R2 TO VSS</td>
<td>Resistor R2 Connection</td>
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<tr>
<td>13</td>
<td>PHASE COMP II OUT</td>
<td>Phase Comparator 2 Output</td>
</tr>
<tr>
<td>14</td>
<td>SIGNAL IN</td>
<td>Signal Input</td>
</tr>
<tr>
<td>15</td>
<td>ZENER</td>
<td>Diode Zener</td>
</tr>
<tr>
<td>8</td>
<td>VSS</td>
<td>Negative Supply Voltage</td>
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<tr>
<td>16</td>
<td>VDD</td>
<td>Positive Supply Voltage</td>
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FUNCTIONAL DIAGRAM

ABSOLUTE MAXIMUM RATINGS

<table>
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<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Value</th>
<th>Unit</th>
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<tbody>
<tr>
<td>$V_{DD}$</td>
<td>Supply Voltage</td>
<td>-0.5 to +22</td>
<td>V</td>
</tr>
<tr>
<td>$V_I$</td>
<td>DC Input Voltage</td>
<td>-0.5 to $V_{DD}$ + 0.5</td>
<td>V</td>
</tr>
<tr>
<td>$I_I$</td>
<td>DC Input Current</td>
<td>± 10</td>
<td>mA</td>
</tr>
<tr>
<td>$P_D$</td>
<td>Power Dissipation per Package</td>
<td>200</td>
<td>mW</td>
</tr>
<tr>
<td></td>
<td>Power Dissipation per Output Transistor</td>
<td>100</td>
<td>mW</td>
</tr>
<tr>
<td>$T_{op}$</td>
<td>Operating Temperature</td>
<td>-55 to +125</td>
<td>°C</td>
</tr>
<tr>
<td>$T_{stg}$</td>
<td>Storage Temperature</td>
<td>-65 to +150</td>
<td>°C</td>
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</table>

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. All voltage values are referred to $V_{SS}$ pin voltage.

RECOMMENDED OPERATING CONDITIONS

<table>
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<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Value</th>
<th>Unit</th>
</tr>
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<tbody>
<tr>
<td>$V_{DD}$</td>
<td>Supply Voltage</td>
<td>3 to 20</td>
<td>V</td>
</tr>
<tr>
<td>$V_I$</td>
<td>Input Voltage</td>
<td>0 to $V_{DD}$</td>
<td>V</td>
</tr>
<tr>
<td>$T_{op}$</td>
<td>Operating Temperature</td>
<td>-55 to 125</td>
<td>°C</td>
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## DC SPECIFICATIONS

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<th>Parameter</th>
<th>Test Condition</th>
<th>Value</th>
<th>Unit</th>
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<tbody>
<tr>
<td></td>
<td></td>
<td>V&lt;sub&gt;I&lt;/sub&gt; (V)</td>
<td>V&lt;sub&gt;O&lt;/sub&gt; (V)</td>
<td>T&lt;sub&gt;TA = 25°C&lt;/sub&gt;</td>
</tr>
<tr>
<td></td>
<td></td>
<td>I&lt;sub&gt;IO&lt;/sub&gt; (µA)</td>
<td>V&lt;sub&gt;DD&lt;/sub&gt; (V)</td>
<td>Min.</td>
</tr>
<tr>
<td>V&lt;sub&gt;OH&lt;/sub&gt;</td>
<td>High Level Output Voltage</td>
<td>0/5 &lt;1 5</td>
<td>4.95</td>
<td>4.95</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0/10 &lt;1 10</td>
<td>9.95</td>
<td>9.95</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0/15 &lt;1 15</td>
<td>14.95</td>
<td>14.95</td>
</tr>
<tr>
<td>V&lt;sub&gt;OL&lt;/sub&gt;</td>
<td>Low Level Output Voltage</td>
<td>5/0 &lt;1 5</td>
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<td>0.05</td>
</tr>
<tr>
<td></td>
<td></td>
<td>10/0 &lt;1 10</td>
<td>0.05</td>
<td>0.05</td>
</tr>
<tr>
<td></td>
<td></td>
<td>15/0 &lt;1 15</td>
<td>0.05</td>
<td>0.05</td>
</tr>
<tr>
<td>I&lt;sub&gt;OH&lt;/sub&gt;</td>
<td>Output Drive Current</td>
<td>0/5 2.5 &lt;1 5</td>
<td>-1.36</td>
<td>-3.2</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0/10 4.6 &lt;1 5</td>
<td>-0.44</td>
<td>-1</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0/15 13.5 &lt;1 15</td>
<td>-3</td>
<td>-6.8</td>
</tr>
<tr>
<td>I&lt;sub&gt;OL&lt;/sub&gt;</td>
<td>Output Sink Current</td>
<td>0/5 0.4 &lt;1 5</td>
<td>0.44</td>
<td>1</td>
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<tr>
<td></td>
<td></td>
<td>0/10 0.5 &lt;1 10</td>
<td>1.1</td>
<td>2.6</td>
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<tr>
<td></td>
<td></td>
<td>0/15 1.5 &lt;1 15</td>
<td>3.0</td>
<td>6.8</td>
</tr>
<tr>
<td>I&lt;sub&gt;I&lt;/sub&gt;</td>
<td>Input Leakage Current</td>
<td>0/18 Any Input</td>
<td>18</td>
<td>±10&lt;sup&gt;-5&lt;/sup&gt;</td>
</tr>
<tr>
<td></td>
<td></td>
<td>19/9 Any Input</td>
<td>19</td>
<td>±10&lt;sup&gt;-5&lt;/sup&gt;</td>
</tr>
<tr>
<td>I&lt;sub&gt;OUT&lt;/sub&gt;</td>
<td>High Impedance Leakage Current</td>
<td>0/18 Any Input</td>
<td>18</td>
<td>±10&lt;sup&gt;-4&lt;/sup&gt;</td>
</tr>
<tr>
<td>C&lt;sub&gt;I&lt;/sub&gt;</td>
<td>Input Capacitance</td>
<td>Any Input</td>
<td>5</td>
<td>7.5</td>
</tr>
</tbody>
</table>

The Noise Margin for both "1" and "0" level is: 1V min. with V<sub>DD</sub>=5V, 2V min. with V<sub>DD</sub>=10V, 2.5V min. with V<sub>DD</sub>=15V
## ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test Condition</th>
<th>Value (*)</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>PD</td>
<td>Operating Power Dissipation</td>
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<tr>
<td></td>
<td></td>
<td>V_{DD} (V)</td>
<td>Min. Typ. Max.</td>
<td>µW</td>
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<tr>
<td></td>
<td></td>
<td>5</td>
<td>10</td>
<td>15</td>
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<tr>
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<td></td>
<td>10</td>
<td>800</td>
<td>1600</td>
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<td>15</td>
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<td>140</td>
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<tr>
<td>f_{MAX}</td>
<td>Maximum frequency</td>
<td></td>
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<tr>
<td></td>
<td></td>
<td>V_{COIN} = V_{DD}/2</td>
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</tr>
<tr>
<td></td>
<td></td>
<td>5</td>
<td>0.3</td>
<td>0.6</td>
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<td>10</td>
<td>0.6</td>
<td>1.2</td>
</tr>
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<td>15</td>
<td>0.8</td>
<td>1.6</td>
</tr>
<tr>
<td></td>
<td></td>
<td>V_{COIN} = V_{DD}</td>
<td></td>
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<tr>
<td></td>
<td></td>
<td>5</td>
<td>0.5</td>
<td>0.8</td>
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<td></td>
<td></td>
<td>10</td>
<td>1</td>
<td>1.4</td>
</tr>
<tr>
<td></td>
<td></td>
<td>15</td>
<td>1.4</td>
<td>2.4</td>
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<tr>
<td>f_{MIN}</td>
<td>Center Frequency (f_{O}) and frequency Range f_{MAX} - f_{MIN}</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Programable with external components R_1, R_2, and C_1</td>
<td></td>
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</tr>
<tr>
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</tr>
<tr>
<td>Linearity</td>
<td></td>
<td>V_{COIN} = 2.5V^{0.3}</td>
<td>R_{1} = 10KΩ</td>
<td>1.7</td>
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<td>10</td>
<td>V_{COIN} = 5V^{1.1}</td>
<td>R_{1} = 100KΩ</td>
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<td>10</td>
<td>V_{COIN} = 5V^{2.5}</td>
<td>R_{1} = 400KΩ</td>
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<td>15</td>
<td>V_{COIN} = 7.5V^{1.5}</td>
<td>R_{1} = 100KΩ</td>
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<td></td>
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<td>15</td>
<td>V_{COIN} = 7.5V^{5}</td>
<td>R_{1} = 1MΩ</td>
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<tr>
<td>f_{MIN}</td>
<td>Temperature Frequency Stability (no frequency offset) f_{MIN} = 0</td>
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<td>±0.12</td>
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</tr>
<tr>
<td></td>
<td></td>
<td>10</td>
<td>±0.04</td>
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<td></td>
<td></td>
<td>15</td>
<td>±0.015</td>
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<tr>
<td>f_{MIN}</td>
<td>Temperature Frequency Stability (frequency offset) f_{MIN} = 0</td>
<td></td>
<td>±0.09</td>
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</tr>
<tr>
<td></td>
<td></td>
<td>10</td>
<td>±0.07</td>
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<td></td>
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<td>15</td>
<td>±0.03</td>
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<tr>
<td>VCO</td>
<td>Output Duty Cycle</td>
<td>5, 10, 15</td>
<td>50</td>
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<td>f_{TLH}</td>
<td>VCO Output Transition Time</td>
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<td>100</td>
<td>200</td>
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<td></td>
<td></td>
<td>10</td>
<td>50</td>
<td>100</td>
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<td></td>
<td>15</td>
<td>40</td>
<td>80</td>
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<tr>
<td>RS</td>
<td>Source Follower Output (Demodulated Output): Offset Voltage V_{COIN}-V_{DEM}</td>
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<td>1.8</td>
<td>2.5</td>
</tr>
<tr>
<td></td>
<td></td>
<td>5, 10, 15</td>
<td>R_{S} &gt; 10KΩ</td>
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</tr>
<tr>
<td>RS</td>
<td>Source Follower Output (Demodulated Output): Linearity</td>
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<td>0.3</td>
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<tr>
<td></td>
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<td>5</td>
<td>V_{COIN} = 2.5V^{0.3}</td>
<td>R_{S} = 100KΩ</td>
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<td></td>
<td>10</td>
<td>V_{COIN} = 5V^{2.5}</td>
<td>R_{S} = 300KΩ</td>
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<td>15</td>
<td>V_{COIN} = 7.5V^{5}</td>
<td>R_{S} = 500KΩ</td>
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<td>V_Z</td>
<td>Zener Diode Voltage</td>
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<td>4.45</td>
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<td></td>
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<td>5</td>
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### PHASE COMPARATOR SECTION

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<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test Condition</th>
<th>Value (*)</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>V_{DD} (V)</td>
<td>Min.</td>
<td>Typ.</td>
<td>Max.</td>
<td></td>
</tr>
<tr>
<td>R14</td>
<td>Pin 14 (signal in)</td>
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<td>AC Coupled Signal</td>
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<td>Input Sensivity (*)</td>
<td>(peak to peak)</td>
<td>5</td>
<td>( f_{IN} = 100\text{KHz} ) sine wave</td>
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<td>t\text{PHZ}</td>
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<td>t\text{PLZ}</td>
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<td>5</td>
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<td>t_{TLH}, t_{THL}</td>
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(*) For sine Wave the frequency must be greater than 10KHz for Phase Comparator II
**DESIGN INFORMATION** This information is a guide for approximating the value of external components in a Phase-Locked-Loop system. The selected external components must be within the following ranges:

\[
5 \text{K} \Omega \leq R_1, R_2, R_S \leq 1 \text{M} \Omega \quad C_1 \geq 100 \text{pF at } V_{DD} \geq 5 \text{V} \quad C_1 \geq 50 \text{pF at } V_{DD} \geq 10 \text{V}
\]

For further information, see

(2) G.S. Mosckytz "miniaturized RC filters using phase Lockedloop" BSTJ May 1965

---

<table>
<thead>
<tr>
<th>CHARACTERISTICS</th>
<th>USING PHASE COMPARATOR I</th>
<th>USING PHASE COMPARATOR II</th>
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<tr>
<td></td>
<td>VCO WITHOUT OFFSET R2=\infty</td>
<td>VCO WITHOUT OFFSET R2=\infty</td>
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<td>VCO Frequency</td>
<td><img src="image1" alt="Diagram" /></td>
<td><img src="image2" alt="Diagram" /></td>
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<td>For No Signal Input</td>
<td>VCO in PLL System will Adjust to Centre Frequency ( f_0 )</td>
<td>VCO in PLL System will Adjust to Lowest Operating Frequency ( f_0 )</td>
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<tr>
<td>Frequency Lock Range, ( 2f_L )</td>
<td>( 2f_L = \text{Full VCO Frequency Range} )</td>
<td>( 2f_L = f_{max} - f_{min} )</td>
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<tr>
<td>Frequency Lock Range, ( 2f_C )</td>
<td><img src="image4" alt="Diagram" /></td>
<td><img src="image5" alt="Diagram" /></td>
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<tr>
<td>Loop filter Component Section</td>
<td><img src="image6" alt="Diagram" /></td>
<td><img src="image7" alt="Diagram" /></td>
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<tr>
<td>Phase Angle Between Signal and Comparator</td>
<td>90° at Centre frequency ( f_C ), approximating 0° and 180° at ends of lock range (2 ( f_L ))</td>
<td>Always 0° in lock</td>
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<td>Locks on Harmonics of Centre Frequency</td>
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<td>Signal Input Noise Rejection</td>
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For further information, see

(2) G.S. Mosckytz “miniaturized RC filters using phase Lockedloop” BSTJ May 1965
Plastic DIP-16 (0.25) MECHANICAL DATA

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<tr>
<td>I</td>
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### SO-16 MECHANICAL DATA

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<td>8° (max.)</td>
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**Diagram:**

- Dimensions: A, a1, a2, b, b1, C, c1, D, E, e, e3, F, G, L, M.
- Orientation: Top view and side view.

*PO13H*